The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor memory element ~~characterized by~~ comprising a semiconductor activating layer comprising a channel region and one conductive type impurity region, a first gate insulating film, a charge accumulating layer, a second gate insulating film, and a control gate electrode,

wherein the semiconductor memory element is formed over a substrate having an insulating surface;

wherein the semiconductor activating layer includes a metal element;

wherein the channel region is a polycrystal semiconductor film crystallized by being continuously scanned at least in the same channel region in irradiating a laser beam; and

wherein a grain boundary of a crystal grain ~~constituting~~ in the polycrystal semiconductor film is flat or formed with a recessed portion.

2. (Currently Amended) A semiconductor memory element ~~characterized by~~ comprising a semiconductor activating layer comprising a channel region and one conductive type impurity region, a first gate insulating film, a charge accumulating layer, a second gate insulating film, and a control gate electrode,

wherein the semiconductor memory element is formed over a substrate having an insulating surface;

wherein the semiconductor activating layer includes a metal element;

wherein the semiconductor activating layer is a polycrystal semiconductor film constituted by aggregating a plurality of crystal grains elongated in the same direction; and

wherein a grain boundary of the crystal grain constituting the polycrystal semiconductor film is flat or formed with a recessed portion.

3. (Currently Amended) A semiconductor memory element ~~characterized by~~ comprising a semiconductor activating layer comprising a channel region and one conductive type impurity region, a first gate insulating film, a charge accumulating layer, a second gate insulating film, and a control gate electrode,

wherein the semiconductor memory element is formed over a substrate having an insulating surface;

wherein the semiconductor activating layer includes a metal element;

wherein the channel region is a polycrystal semiconductor film crystallized by being continuously scanned at least in the same channel region in irradiating a laser beam; and

wherein a surface roughness of the channel region is 0.1 nm through 60nm in a P-V value.

4. (Currently Amended) A semiconductor memory element ~~characterized by~~ comprising a semiconductor activating layer comprising a channel region and one conductive type impurity region, a first gate insulating film, a charge accumulating layer, a second gate insulating film, and a control gate electrode;

wherein the semiconductor memory element is formed over a substrate having an insulating surface,

wherein the semiconductor activating layer includes a metal element;

wherein the semiconductor activating layer is a polycrystal semiconductor film constituted by aggregating a plurality of crystal grains elongated in the same direction; and

wherein a surface roughness of the channel region is 0.1 nm through 60 nm in a P-V value.

5. (Currently Amended) A semiconductor memory element ~~characterized by~~ comprising a semiconductor activating layer comprising a channel region and one conductive type impurity region, a first gate insulating film, a charge accumulating layer, a second gate insulating film, and a control gate electrode,

wherein the semiconductor memory element is formed over a substrate having an insulating surface;

wherein the semiconductor activating layer includes a metal element;

wherein the channel region is a polycrystal semiconductor film crystallized by being continuously scanned at least in the same channel region in irradiating a laser beam; and

wherein a surface roughness of the channel region is 0.1 nm through 5 nm in [[a]] an rms value.

6. (Currently Amended) A semiconductor memory element ~~characterized by~~ comprising a semiconductor activating layer comprising a channel region and one conductive type impurity region, a first gate insulating film, a charge accumulating layer, a second gate insulating film, and a control gate electrode,

wherein the semiconductor memory element is formed over a substrate having an insulating surface;

wherein the semiconductor activating layer includes a metal element;

wherein the semiconductor activating layer is a polycrystal semiconductor film constituted by aggregating a plurality of crystal grains elongated in the same direction; and

wherein a surface roughness of the channel region is 0.1 nm through 5 nm in [[a]] an rms value.

7. (Currently Amended) The semiconductor memory element according to any one of claim 1 through claim 6, ~~characterized in that~~ wherein a concentration of the metal element falls in a range of $1 \times 10^{16}/cm^3$ through $5 \times 10^{18}/cm^3$.

8. (Currently Amended) The semiconductor memory element according any one of claim 1 through claim 6, ~~characterized in that~~ wherein the semiconductor activating layer is the polycrystal semiconductor film subjected to a heating treatment and adding the metal element.

9. (Currently Amended) The semiconductor memory element according to any one of claim 1 through claim 6, ~~characterized in that~~ wherein the metal element is one kind or a plurality of kinds selected from the group consisting of Fe, Ni, Co, Ge, Sn, Pd, Pt, Cu, and Au.

10. (Currently Amended) The semiconductor memory element according to any one of claim 1 through claim 6, ~~characterized in that~~ wherein a channel length of the semiconductor memory element is 0.01 μm through 2 μm.

11. (Currently Amended) A semiconductor memory device ~~characterized by,~~ further including a memory cell array arranged with the semiconductor memory element according to any one of claim 1 through claim 6 in a shape of a matrix.

12. (Currently Amended) A semiconductor memory device, wherein a memory cell array arranged with the semiconductor memory element according to any one of claim 1 through claim 6 in a shape of a matrix is formed on a plastic substrate or a ceramic substrate.

13. (Currently Amended) A semiconductor memory device ~~characterized by,~~ including an IC chip constituted by laminating an involatile memory having a memory cell array arranged with the semiconductor memory element according to any one of claim 1 through claim 6 in a shape of a matrix.

14. (Currently Amended) A semiconductor memory device ~~characterized in that,~~ wherein the semiconductor memory device according to any one of claim 1 through claim 6 is one selected from a game machine, a video camera, a head attaching type display, a DVD player, a personal computer, a portable telephone, and a car audio.

15.-16. (Canceled)

17. (New) A semiconductor memory element comprising a semiconductor activating layer comprising a channel region and one conductive type impurity region, a first gate insulating film, a charge accumulating layer, a second gate insulating film, and a control gate electrode,

wherein the semiconductor memory element is formed over a substrate having an insulating surface;

wherein the semiconductor activating layer includes a metal element;

wherein the channel region is a crystallized polycrystal semiconductor film; and

wherein a grain boundary of a crystal grain in the polycrystal semiconductor film is flat or formed with a recessed portion.

18. (New) A semiconductor memory element comprising a semiconductor activating layer comprising a channel region and one conductive type impurity region, a first gate insulating film, a charge accumulating layer, a second gate insulating film, and a control gate electrode,

wherein the semiconductor memory element is formed over a substrate having an insulating surface;

wherein the semiconductor activating layer includes a metal element;

wherein the channel region is a crystallized polycrystal semiconductor film; and

wherein a surface roughness of the channel region is 0.1 nm through 60nm in a P-V value.

19. (New) A semiconductor memory element comprising a semiconductor activating layer comprising a channel region and one conductive type impurity region, a first gate insulating film, a charge accumulating layer, a second gate insulating film, and a control gate electrode,

wherein the semiconductor memory element is formed over a substrate having an insulating surface;

wherein the semiconductor activating layer includes a metal element;

wherein the channel region is a crystallized polycrystal semiconductor film; and

wherein a surface roughness of the channel region is 0.1 nm through 5 nm in an rms value.

20. (New) The semiconductor memory element according to any one of claim 17 through claim 19, wherein a concentration of the metal element falls in a range of $1 \times 10^{16}/cm^3$ through $5 \times 10^{18}/cm^3$.

21. (New) The semiconductor memory element according any one of claim 17 through claim 19, wherein the semiconductor activating layer is the crystallized polycrystal semiconductor film subjected to a heating treatment and adding the metal element.

22. (New) The semiconductor memory element according to any one of claim 17 through claim 19, wherein the metal element is one kind or a plurality of kinds selected from the group consisting of Fe, Ni, Co, Ge, Sn, Pd, Pt, Cu, and Au.

23. (New) The semiconductor memory element according to any one of claim 17 through claim 19, wherein a channel length of the semiconductor memory element is 0.01 μm through 2 μm.

24. (New) A semiconductor memory device, further including a memory cell array arranged with the semiconductor memory element according to any one of claim 17 through claim 19 in a shape of a matrix.

25. (New) A semiconductor memory device, wherein a memory cell array arranged with the semiconductor memory element according to any one of claim 17 through claim 19 in a shape of a matrix is formed on a plastic substrate or a ceramic substrate.

26. (New) A semiconductor memory device, including an IC chip constituted by laminating an involatile memory having a memory cell array arranged with the semiconductor memory element according to any one of claim 17 through claim 19 in a shape of a matrix.

27. (New) A semiconductor memory device, wherein the semiconductor memory device according to any one of claim 1 through claim 6 is one selected from a game machine, a video camera, a head attaching type display, a DVD player, a personal computer, a portable telephone, and a car audio.